OrCAD
CADENCE PCB SOLUTIONS

FEATURE	Standard	Professional	Allegro
Floating Networked License	✓	✓	✓
12 Months Maintenance Support Included In Purchase Price	✓	✓	✓
SCHEMATIC ENTRY + DATA MANAGEMENT	Standard	Professional	Allegro
Flexible Window layout	✓	✓	✓
Graphical, flat and hierarchical page editor and Picture block hierarchy	✓	✓	✓
OrCAD PSpice AD Basics - Restricted Capacity see PSpice matrix below	✓	✓	Allegro PSpice System Designer
Net Groups - Complex bus definition	✓	✓	✓
AutoWire	✓	✓	✓
44,000 Schematic symbols	✓	✓	✓
Coloured Components / nets	✓	✓	✓
Tcl TK scripting support	✓	✓	✓
Online design rule check including custom DRC capability and Waive DRC	✓	✓	✓
Forward and back-annotation of properties / pin-and-gate swaps	✓	✓	✓
Schematic Part and Library editor	✓	✓	✓
Cross-probing and cross-placing	✓	✓	✓
FPGA design-in / pin import & export			
Multiple PCB netlist interfaces - New Design Sync for Cadence Flow	✓	✓	✓
Part Search Providers UltraLibrarian and Samcsys (Symbol, Footprint 3d Step Mode	✓	✓	✓
Property editor for pins, components, nets	✓	✓	✓
OrCAD SigXplorer SI Analysis	✓	✓	✓
Intelligent PDF creation	✓	✓	✓
Advanced Annotation	✓	✓	✓
Design Compare (detail and Graphical)	✓	✓	✓
Default Demo designs	✓	✓	✓
Extended Preferences	✓	✓	✓
Export ISCF (Intel Schematic Connectivity Format)	✓	✓	✓
Export / Import XML	✓	✓	✓
Altium Importer Schematic (PCB also available)	✓	✓	✓
Eagle Importer Schematic (PCB also available)	✓	✓	✓
Constraint Manager	✓	✓	✓
Component Information System	CIS option	CIS option	✓
Windows ODBC compatible format	CIS option	CIS option	✓
Interface to relational database and management systems	CIS option	CIS option	✓
Database query for part selection and parametric properties	CIS option	CIS option	✓
Schematic and BOM Variants Manager (Parts not Fitted and more).	CIS option	CIS option	✓
Component Information Portal (CIP), Access to Mouser, Digikey, Future, Farnell	CIS Option + CIP E Option	CIS Option + CIP E Option	CIP E Option
PCB EDITOR	Standard	Professional	Allegro
Spacing, Same net, Netclass and Class to Class rules	✓	✓	✓
Physical Constraint Rules	✓	✓	✓
DesignTrue DFM Wizard	✓	✓	✓
Design for Test Checks	✓	✓	✓
Design For Assembly Checks	✓	✓	✓
Design For Fabrication Checks	✓	✓	✓
Version Control	✓	✓	✓
Component Lead Editor	✓	✓	✓
Import File Manager	✓	✓	✓
DFM Pad Entry / Exit Rules	✓	✓	✓
Dynamic pad suppression / Unused Pad removal	✓	✓	✓
Cross Section Editor	✓	✓	✓
Padstack Editor IPC2581 Compliant	✓	✓	✓
Application Mode (General, Etch, Placement)	✓	✓	✓
Application Mode (shape)	✓	✓	✓
Full Skill Support	✓	✓	✓
Customisable Visibility Pane	✓	✓	✓
Dynamic Shape Pin Connection By Layer (Global/Shape/Pin/Layer)	✓	✓	✓
Dynamic Cross Hatch Shapes	✓	✓	✓
Dynamic Shapes (dynamic copper pours) Plow and Heal	✓	✓	✓
Move with autoroute adjust (Slide)	✓	✓	✓
Multiple placement options, manual, quickplace, auto and room	✓	✓	✓
Alignment x and y for components and modules	✓	✓	✓
Dynamic rat suppression	✓	✓	✓
Fan-out generators	✓	✓	✓
Interactive Routing using Working Layer (layer selection popup)	✓	✓	✓
Group route Bus Route and via patterns	✓	✓	✓
Line Fattening	✓	✓	✓
Differential Pair Static Phase Control rules	✓	✓	✓
Differential Pairs Physical rules and routing	✓	✓	✓
Blind Buried Single Click multiple via instantiation	✓	✓	✓
Push, Shove and Hug interactive editing	✓	✓	✓
Curve Routing	✓	✓	✓
Snake Routing for Hex pattern ICs	✓	✓	✓
Auto Finish (Route Completion Tool)	✓	✓	✓
Scribble Sketch Routing	✓	✓	✓
Route cleanup, optimization (Glossing)	✓	✓	✓
Embedded net names	✓	✓	✓
Split View	✓	✓	✓
Through Board Transparency (OpenGL)	✓	✓	✓
Flip Board	✓	✓	✓
Excellon NC Drill File export	✓	✓	✓

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Gerber 274X, 274D artwork Output	✓	✓	✓
IPC2581 Import / Export	✓	✓	✓
Mentor ODB++ and universal viewer	✓	✓	✓
Impedance Calculator	✓	✓	✓
Interactive / Automatic Silkscreen generation	✓	✓	✓
Import Altium PCB (schematic also available)	✓	✓	✓
Import PADS & PCAD	✓	✓	✓
Import IFF RF Shapes	✓	✓	✓
Import Export DXF	✓	✓	✓
Import Export IDF	✓	✓	✓
Export Intelligent PDF	✓	✓	✓
MCAD/ECAD Incremental design data exchange (IDX)	✓	✓	✓
3D/2D Crossprobing	✓	✓	✓
STEP 3D Clash Detect	✓	✓	✓
STEP 3D viewer for selected item or complete PCB.	✓	✓	✓
STEP 3D Canvas Controls	✓	✓	✓
STEP 3D Import Export	✓	✓	✓
STEP 3D Canvas Highlight Selections	✓	✓	✓
Manual Design For Test (DFT) / Test Prep	✓	✓	✓
Associative Dimensioning	✓	✓	✓
Route Nets by Pick, 6- Signal Layers, no layer limit or Pin Limit	✓	✓	✓
Route Automatic, 6- Signal Layers, no layer limit or Pin Limit		✓	✓
Net Scheduling, T-Point rules (pin to T-point), T-Point definition		✓	✓
Constraint Regions, region based rules (Rigid-Flex; BGA regions)		✓	✓
Propagation delay rules (Relative) for nets or groups		✓	✓
Propagation delay rules (Min/Max) for nets or groups		✓	✓
Total Etch Length - Max/Min Length		✓	✓
Extended (X)net rules		✓	✓
Layer set rules		✓	✓
Pin Pair rules		✓	✓
Delay Tuning		✓	✓
Dynamic Heads-up Display for critical rules		✓	✓
Hug Contour routing (Flex)		✓	✓
Segment over void detection		✓	✓
Spread lines between voids		✓	✓
Shape based curve fillet support, tapered traces		✓	✓
Placement replication, template based design reuse		✓	✓
Via array / Shielding - Shape and Trace based		✓	✓
Rigid Flexi Zone Management		✓	✓
Dynamic Zone Placement		✓	✓
Inter Layer Checks for Rigid Flexi		✓	✓
3D Bending		✓	✓
High Speed Analysis Impedance Workflow		✓	✓
High Speed Analysis Coupling Workflow		✓	✓
Placement Vision		✓	✓
Route Vision		✓	✓
Differential Pair Dynamic Phase Control rules		✓	✓
Package Pin Delay (for die-2-die delay) rules		✓	✓
Z-Axis delay feedback		✓	✓
Backdrilling		✓	✓
Automatic Design For Test (DFT) / Test Prep		✓	✓
Panelization		✓	✓
Max Via Count rules			✓
Offset Routing			✓
Design planning - Create hierarchical Bundles			✓
Design planning - Create, Edit Flows			✓
Design planning - Assign Flows to Layers			✓
Dynamic Shape based curve fillet support, tapered traces			✓
CAD Translators - Import Mentor Boardstation			✓
Allegro Constraint Compiler			PCB High-Speed Option
High Speed Return Path DRC			PCB High-Speed Option
High Speed IR Drop Analysis Workflow (load capability)			PCB High-Speed Option
High Speed Reflection Analysis Workflow (load capability)			PCB High-Speed Option
Automatic Delay Tune (AiDT)			PCB High-Speed Option
Automatic Phase Tune (AiPT)			PCB High-Speed Option
Remove Tuning			PCB High-Speed Option
Timing Vision (Coloured tracks based on constraint adherence)			PCB High-Speed Option
Tabbed Routing			PCB High-Speed Option
Electrical Constraint rule set (ECSets) / Topology Apply			PCB High-Speed Option
Electrical rules (Reflection, Timing, Crosstalk)			PCB High-Speed Option
Advanced Constraints (formulas, relational)			PCB High-Speed Option
Fabric Weave Effect Zig Zag Auto Interactive			PCB High-Speed Option
High Speed Static Phase Via Transition DRC			PCB High-Speed Option
Via Voiding Differential Pairs			PCB High-Speed Option
Single net Return Paths Vias			PCB High-Speed Option
High Speed Differential Pair Return Path Vias			PCB High-Speed Option
High Speed Intra Differential Pairs Spacing Rules			PCB High-Speed Option
High Speed Via Structures			PCB High-Speed Option
High Speed Inductance Via Structures			PCB High-Speed Option
Constraint Manager: HDI rule set			Miniaturization Option
Micro-via and associated spacing, stacking and via-in-pad rules			Miniaturization Option
Constraint driven HDI design flow			Miniaturization Option
HDI micro-via stack editing			Miniaturization Option
Manufacturing rule support for embedding components			Miniaturization Option
Embed components on inner layers			Miniaturization Option
Support for Cavities on inner layers			Miniaturization Option

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Support for Vertically placed components on inner layers			Miniaturization Option
Soldermask for embedded components			Miniaturization Option
Support for copy and swap embedded components			Miniaturization Option
Dual Side Contact Embedded Components			Miniaturization Option
Design Planning - Plan Spatial Feasibility analysis & feedback			Design Planning Option
Design Planning - Generate Topological Plan			Design Planning Option
Design Planning - Convert Topological plan to traces (CLINES)			Design Planning Option
Auto Interactive Break-out (AiBT)			Design Planning Option
Auto Connect (Breakout, Connect, Compress, Spread, Nudge, Push)			Design Planning Option
Symphony Team Design New Option, one board with multiple designers in real time			Symphony Team Design Option
Swap pins on a FPGA (based on FPGA rules) in PCB Editor			FPGA System Planner
Reoptimize pins on a FPGA (using FPGA rules)			FPGA System Planner
Parameterized RF etch elements			PCB Analog / RF Option
Asymmetrical Clearances			PCB Analog / RF Option
RF Etch elements editing			PCB Analog / RF Option
Bi-Directional interface with Agilent ADS			PCB Analog / RF Option
Layout-driven RF design creation			PCB Analog / RF Option
Flexible Shape Editor			PCB Analog / RF Option
PSpice SIMULATION	Standard	Professional	Allegro
Bias Point, DC sweep, AC sweep & transient analysis (with Temperature)	PSpice AD	PSpice AD	PSpice AD
Parametric Analysis	PSpice AD	PSpice AD	PSpice AD
Learning PSpice Free Templates	PSpice AD	PSpice AD	PSpice AD
Analog behavioural modelling	PSpice AD	PSpice AD	PSpice AD
Stimulus editor	PSpice AD	PSpice AD	PSpice AD
Model Editor for device characterization	PSpice AD	PSpice AD	PSpice AD
Interactive waveform viewer & analyzer	PSpice AD	PSpice AD	PSpice AD
IBIS / DML model support	PSpice AD	PSpice AD	PSpice AD
Monte Carlo: Statistical circuit behaviour and yield (Worst Case)	PSpice AD	PSpice AD	PSpice AD
Bias point voltages, currents and power display on schematic	PSpice AD	PSpice AD	PSpice AD
Sensitivity: Identifies critical circuit components	Advanced Analysis	Advanced Analysis	Advanced Analysis
Optimizer: Optimizes key circuit components	Advanced Analysis	Advanced Analysis	Advanced Analysis
Monte Carlo: Statistical circuit behaviour and yield multiple measurements	Advanced Analysis	Advanced Analysis	Advanced Analysis
Smoke: Detects component stress	Advanced Analysis	Advanced Analysis	Advanced Analysis
Parametric Plotter: Examine solution through nested sweeps	Advanced Analysis	Advanced Analysis	Advanced Analysis
Optimize Circuits through Curve or Parameter Fit	Advanced Analysis	Advanced Analysis	Advanced Analysis
SIGNAL INTEGRITY	Standard	Professional	Allegro
Pre- & Post-route signal integrity analysis	Pre Route	✓	✓
Graphical topology definition and exploration	Pre Route	✓	✓
Interactive waveform viewer	Pre Route	✓	✓
Macro modelling support (DML)	Pre Route	✓	✓
IBIS 5.0 support	Pre Route	✓	✓
IBIS ICM model support	Pre Route	✓	✓
Spectre-to-DML	Pre Route	✓	✓
HSPICE-to-IBIS	Pre Route	✓	✓
Lossy transmission lines	Pre Route	✓	✓
Coupled (3 net) simulation Pre-Route	Pre Route	✓	✓
Differential pair exploration and simulation	Pre Route	✓	✓
STANDALONE AUTOROUTER	Standard	Professional	Allegro
6 Signal Layers at a time (no board layer limit or pin limit)		✓	✓
Shape-based or Gridded routing		✓	✓
SMD Fanout		✓	✓
Physical Trace Width by Net and Net Classes		✓	✓
45-degree / Memory Pattern Routing		✓	✓
Interactive Routing with Shoving and Plowing		✓	✓
Interactive Floorplanning		✓	✓
Online Design Rule Checking		✓	✓
Flip, Rotate, Align, Push, and Move Components		✓	✓
Placement Density Analysis		✓	✓
Min/Max, matched length rules based autorouting			✓
Pin-pair rules, Area rules based autorouting			✓
Crosstalk controls, parallelism rules based autorouting			✓
Differential Pair Autorouting, Automatic net shielding			✓
High-speed rules-based autorouting			✓
256 signal layer limit		OrCAD AI Option	PCB AutoRouting Option
DFM rules-based autorouting automatic trace spreading, via reduction and mitering			PCB AutoRouting Option
Spacing Net Class - Class Rules			PCB AutoRouting Option
Via Rules by Net and Net Class			PCB AutoRouting Option
Mircovia features including Plural and Stacked microvias			PCB AutoRouting Option
Auto Test Point Generation and Clearance Rules			PCB AutoRouting Option
Layer-specific rules-based autorouting			PCB AutoRouting Option