cadence LIVE EUROPE

Tuesday, 19 October, 2021 - All Times CEST

SUBJECT TO CHANGE

START TIME (CEST)	CUSTOM AND ANALOG DESIGN - I	CUSTOM AND ANALOG DESIGN - I I	MIXED-SIGNAL DESIGN - I	MIXED-SIGNAL DESIGN - I I	RF DESIGN	DIGITAL IMPLEMENTATION AND SIGNOFF	VERIFICATION	PCB DESIGN AND IC PACKAGING	SYSTEM DESIGN AND ANALYSIS	AUTOMOTIVE AND IP	ACADEMIC AND ENTREPRENEUR SHOWCASE	CLOUD	COMPUTATIONAL FLUID DYNAMICS
KEYNOTES													
9:30	Harnessing the Power of Analytics to Drive the Electronics Industry Renaissance — Lip-Bu Tan, CEO, Cadence												
10:00	Accelerating System Design and Analysis — Dr. Anirudh Devgan, President, Cadence												
11:00	Ericsson Performance for 5G and Beyond — Erik Ekudden, CTO, Ericsson												
11:45	**CADENCE** Cadence Virtuoso and Spectre Technology Update		**INTEL** Mixed-Signal Physical Design for Advanced Nodes Technologies Using OA Based P&R Tool	**STMICROELECTRONICS** Active Filtering Based on EEnet Technology	**CADENCE** AWR Technology Update – Analysis and Work Flow Integration for Advanced RF Systems	**CADENCE** Digital Design and Implementation 2021 Updates	**ARM** De-Risking and Accelerating OS Boot for Arm SystemReady SoCs: A Morello Case Study	**CADENCE** System Design Platform Technology Update – Pervasive Performance and Productivity	**FRAUNHOFER IIS/EAS** A Reference Flow for Chip-Package Co-Design for 5G/mmWave Using Assembly Design Kit (ADK)	**RENESAS** Digital Safety Focused Verification for ISO 26262	**EUROPRACTICE** Updated Cadence Portfolio Available for European Academics via Europractice	**AWS** Accelerating EDA Productivity: The Why, What, and How of the Journey to the Cloud	**UNIVERSITY OF STUTTGART** A High-Quality Automated Meshing Tool for Wind Turbine Blades
12:20			**FRAUNHOFER IIS/EAS** Automation and Reuse of Analog/Mixed-Signal RF Layout Components in Nanometer Nodes	**TEXAS INSTRUMENTS** Are We Done Yet? How to Get an Overview on the Status of the Analog Verification	**CADENCE** Virtuoso RF Solution Technology Update	**SAMSUNG** Differentiated and High Quality Library Solutions Using Liberate Trio	**INFINEON** Improving Simulation Regression Efficiency Using Xcelium Machine Learning Technology in Functional Verification	**STMICROELECTRONICS** A Journey Around ST Automotive Design Evolution and Cadence Platform Solution	**CADENCE** Reimagining 3D FEM Extraction with Clarity 3D Solver	**INFINEON** Evaluation of Legato Reliability Solution in Relation to Practical Aspects of Analog Defect Simulation Applicability in Industry	**OXFORD UNIVERSITY** End-to-End Formal Verification of a Capability Hardware-Enhanced RISC-V Processor	**CADENCE** Cloud-Scale Productivity Without the Complexity—Have Your Cake and Eat It, Too	**FINOT-CONQ** Sailing Cadence FINE/Marine Around the Globe - CFD Simulations at finot-conq for the Vendee Globe 2024
12:55	**STMICROELECTRONICS** From the Best Usage of Advanced Virtuoso Functionalities	**MELEXIS TECHNOLOGIES** Analog Fault Injection for Functional Safety Analysis Using Legato Reliability Solution	**INTEL** Improvement of Productivity for MS Physical Design Implementation by Embedding a P&R Routing Engine into the Analog Design Environment	**RENESAS** Unified Testbench for AMS, DMS and Schematic	**STMICROELECTRONICS** 77 GHz 28FDSOI LNA Full EM Characterization Through Virtuoso RF and EMX	**FRAUNHOFER IIS** How to Handle Successfully the Hierarchical Implementation of a 14M Instance RISC-V Based HPC Design in 22nm FD-SOI	**BROADCOM** Achieving Code Coverage Signoff on a Configurable and Constantly Changing Design Using JasperGold Coverage Unreachability App	**INFINEON** Automatic Verification and Report Generation for Daisy-Chain Test Structures in a Chip/Package/PCB Co-Design Environment	**GRASS VALLEY** System Analysis of a Transmission Board Using Sigrity PowerDC and BBS Tool	**CADENCE** High-Speed 112G Designs and Channel Operating Margin (COM) Dependencies	**DELFT UNIVERSITY OF TECHNOLOGY** A 16-Channel CMOS Reconfigurable Recording Unit for Simultaneous In-Vitro Microelectrode Array (MEA) and Current-Clamp Measurements	**AZURE / D-MATRIX** Developing Scalable AI Inference Chip with Cadence Flow in Azure Cloud	**NUMECA / CADENCE** How Computational Fluid Dynamics Extends Cadence's Multiphysics System Analysis and Design
13:30	Designer Expo												
14:30	**X-FAB** Introduction to an Automated PDK Verification Flow: "XVerifFlow"	**GLOBALFOUNDRIES** Electro-Thermal Co-Simulation for Electromigration Analysis with Voltus-Fi	**CADENCE** Mixed-Signal Verification Technology Update – Advanced Debug Capabilities and Performance Boost		**EXTOLL** On-Chip Inductor Synthesis	**IMEC / CADENCE** Memory-on-Logic Stacking for Multi-Core SoCs at Advanced Nodes	**RC MODULE** Accelerating Simulation of ATPG Scan Tests with Xcelium Multi-Core	**STMICROELECTRONICS** How to Reduce Design Error Risks for Complex 3D BGA/LGA Package Module	**CADENCE** Modelling and Simulation of Differential Chip to PCB Interface up to 40GHz Using 3D-FEM Solver	**CADENCE** Accelerating Automotive Connectivity from Infotainment to ADAS with PCI Express	**NANUSENS** MEMS Sensors Can Now Be Made in Huge Volumes Using CMOS **SPIDEN** A Multi-Modal ASIC for the Continuous Monitoring of Biomarkers and Drugs	**GOOGLE** Designing Planet-Scale Video Chips on Google Cloud	**NUMECA / CADENCE** Omnis, from Meshing to Solving to Optimization, in One Single Multiphysics Environment
15:05	**AMS** A Novel Approach of Integrated Electro-Thermal Simulation for Automotive Applications	**STMICROELECTRONICS** FLUID PCELL: A New Way to Create Layout			**RAMON LLULL UNIVERSITY** Matching Network Synthesis for Virtual Antenna Technology with Microwave Office	**ARM** Energy-Efficient 5nm High-Performance Arm Core Implementation	**STMICROELECTRONICS** Verifying Register Maps with JasperGold CSR: How Formal Compares to UVM	**FLOWCAD** Improving Design Productivity in Allegro and OrCAD PCB Editor Technologies		**FRAUNHOFER IIS/EAS** FIFO-Based Complex-FFT Architectures in Tensilica ConnX B20	**SEMRON** SEMRON´s First Tapeout for Future AI Chips **EQUAL1 LABS** A 22nm FD-SOI-CMOS Scalable Quantum Processor SoC with Fully Integrated Control Electronics at 3.5K		**POINTWISE / CADENCE** Pointwise - The Choice for CFD Meshing
15:40	**STMICROELECTRONICS** A Novel Verification Methodology to Predict Temperature Behaviour of Analog Trimmed Parameters Using Virtuoso ADE and Spectre Simulator	**GLOBALFOUNDRIES** Selfheat Management of 22FDX MMW Design	**RENESAS** Getting Your $$$ from Verilog-A	**MATHWORKS** Rapid Design and Verification of Mixed-Signal Systems Through Virtuoso Suite and MATLAB Integration		**STMICROELECTRONICS** A Vectorless-Based Ecosystem for Voltage-Sensitive Critical Path Identification	**U-BLOX** Emulation as Verification Speedup Platform	**CADENCE** Accelerating PCB Design Cycles with In-Design Analysis		**LEIBNIZ UNIVERSITY HANNOVER** Evaluation of Different ASIP-Configurations for an Embedded Computed Order Tracking Algorithm	**MINRES TECHNOLOGIES** Trustworthy Software-Driven Hardware for the Intelligent Edge **SEAMLESS WAVES** A 1.5-to-3.0GHz Tunable RF Bandpass Sigma-Delta ADC		
16:15	**IC MASK DESIGN** Common Denominator Tiles (CDT) and Embedded Metal Lines (EML)	**INTEL** Aging Profile Simulations with Virtuoso ADE		**X-FAB** Liberate MX Evaluation for CCS, CCSP, CCSN Characterization of X-FAB RAMs and ROMs			**INTEL** Efficient System Stress and Randomization Through PSS Based Concurrency			**ARM** Arm FMEDA Methodology for SEooC IP in Safety-Critical Applications			